Configuration Elements

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Introduction

Altera ensures the highest level of device performance and reliability by maintaining a comprehensive testing program that carefully monitors the factors affecting the basic programming elements of Altera® programmable logic devices (PLDs). Altera PLDs incorporate three types of configuration elements: EEPROM, SRAM, and EPROM.

EEPROM Configuration Element

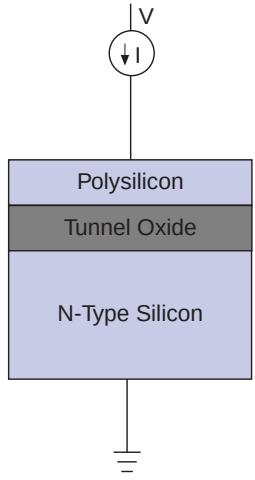
The basic programming element of MAX® 9000 and MAX 7000 devices is the EEPROM cell. The EEPROM transistor is an MOS transistor that is either on or off, depending on the threshold voltage. Unlike EPROM devices, however, EEPROM devices can be erased electrically. The EEPROM cell consists of a single, floating polysilicon gate structure that is used to change the threshold voltage of the transistor. The threshold voltage is changed when a tunneling mechanism traps an excess of electrons on the floating gate. Fowler-Nordheim tunneling occurs when the floating gate is raised to a high voltage (12 V to 13 V) via capacitive coupling to the n+ implant region. Once the electrons have been trapped on the floating gate, they present a negative shielding voltage and increase the threshold voltage of the transistor, making it impossible to turn the transistor on under normal operating voltages. This process allows the floating gate to act as an on / off switch for the read transistor.

The EEPROM cell is erased by the tunneling mechanism. That is, electrons are removed from the floating gate, and the gate has a net positive charge that allows the EEPROM transistor to be turned on or off, depending on the voltage on the control gate.

For a complete operational description of the EEPROM cell, see the *Altera Reliability Report*, which is available from Altera Literature Services or your local sales representative.

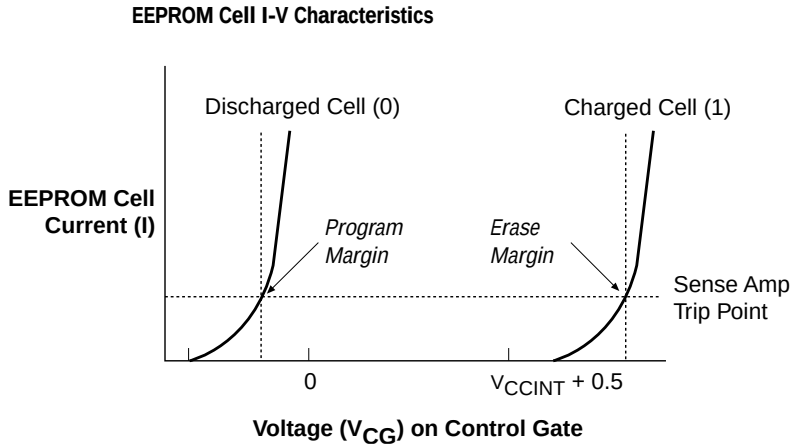
Figure 1 shows a 2-electrode structure in which one electrode is formed by polysilicon and another is formed by a heavily doped N-type silicon diffusion. These electrodes are separated by a tunnel oxide. When typical operating voltages of 5 V or less are applied across the tunnel oxide, it acts as a dielectric and does not conduct electricity. When 12 V to 14 V are applied, however, electrons tunnel through the oxide. This process is characterized by an extremely small tunneling current (less than 10^{-20} A) at typical operating voltages of 5 V or less. At the higher voltages used to erase or program the cell (i.e., charge or discharge the floating gate), the exponential rise in current produces approximately 1 µA of current flow through the tunnel oxide. Depending on the voltage's polarity, this current is sufficient to charge or discharge the cell within a few milliseconds.

Figure 1. EEPROM Floating-Gate Electrode, Tunnel Oxide & Heavily Doped Diffusion Electrode



The I-V relationships are shown in Figure 2. Unlike the EPROM cell, the threshold voltage of a discharged EEPROM cell is negative (less than 0 V) because electrons are removed from the floating gate. Electron removal gives the floating gate a net positive charge.

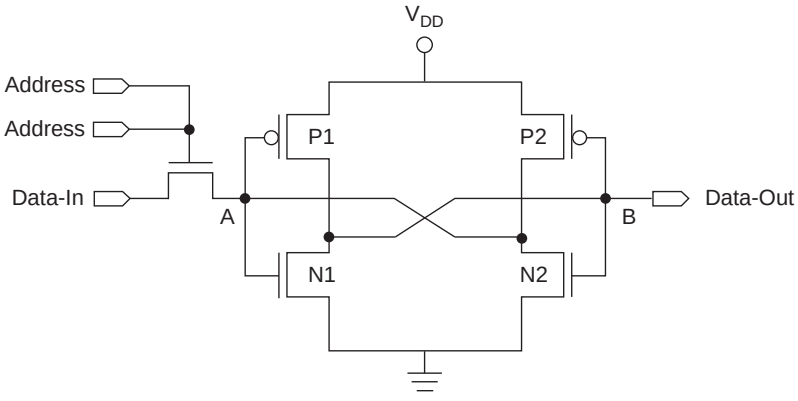
Figure 2. Current vs. Voltage Relationships of EEPROM Cells



SRAM Configuration Element

The basic programming elements of Altera's FLEX® 10K, FLEX 8000, and FLEX 6000 PLDs are SRAM configuration elements. Figure 3 shows the standard CMOS five-transistor cell that comprises the configuration element.

Figure 3. SRAM Configuration Element



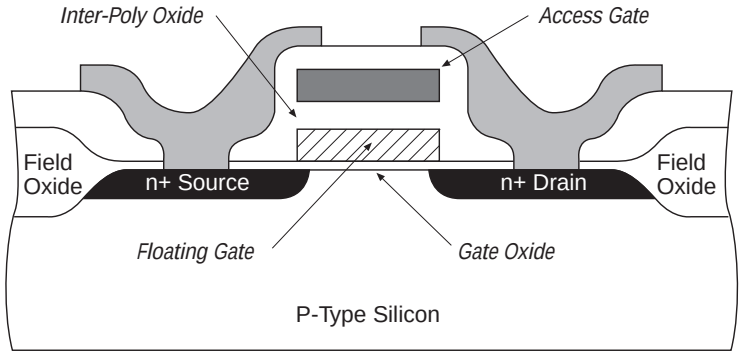
The FLEX 10K, FLEX 8000, and FLEX 6000 device manufacturing process is a subset of the EEPROM fabrication process. Therefore, all development and reliability enhancements used to manufacture EEPROM devices also apply to SRAM-based devices.

EPROM Configuration Element

The basic programming elements of MAX 5000 and Classic™ devices are EPROM configuration elements. The EPROM transistor is a modified NMOS transistor in which the threshold voltage is easily switched between a low voltage (near V_{SS}) and a high voltage (greater than V_{CC}). The different threshold voltages represent the EPROM cell in the on and off states.

The EPROM transistor has a floating polysilicon gate between the access gate and the substrate, as shown in Figure 4. The floating gate is electrically isolated from the substrate by a thin gate oxide, and from the access gate by a thicker dielectric inter-poly oxide that typically consists of oxides and / or nitrides.

Figure 4. EPROM Cell Construction



EPROM transistors are programmed to a high-threshold voltage with hot electron injection. When a high programming voltage (V_{PP}) is applied to the access gate of an EPROM cell, and a slightly lower voltage (V_D) is applied to its drain, electrons flow from the source to the drain. As these electrons pick up kinetic energy, their path is altered by an electric field located between the access gate and substrate. This electric field is generated by the potential difference between V_{PP} on the access gate and V_D on the drain. Electrons that achieve a kinetic energy of 3.2 eV accelerate vertically toward the floating gate, pass through the gate oxide, and are trapped on the floating-gate electrode. These electrons create a net negative voltage on the floating gate that opposes the electrical field created by the positive voltage on the access gate. The result is a substantial increase in the threshold voltage required to change the EPROM cell from a non-conducting to a conducting state. See Figure 5.

Figure 5. EPROM Cell Programming

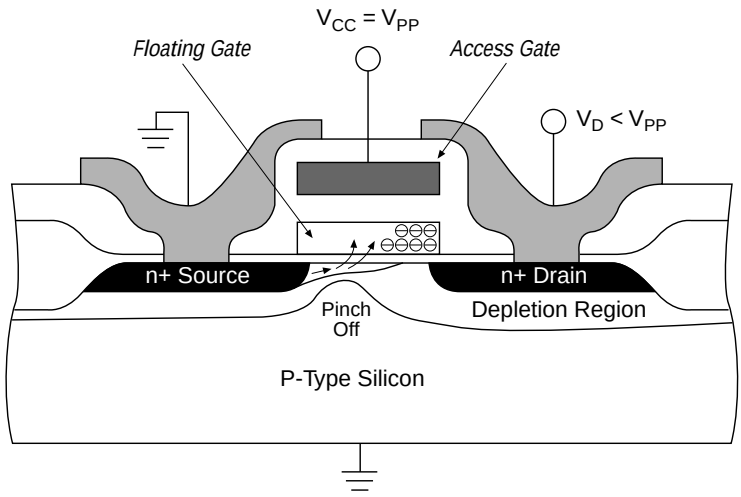
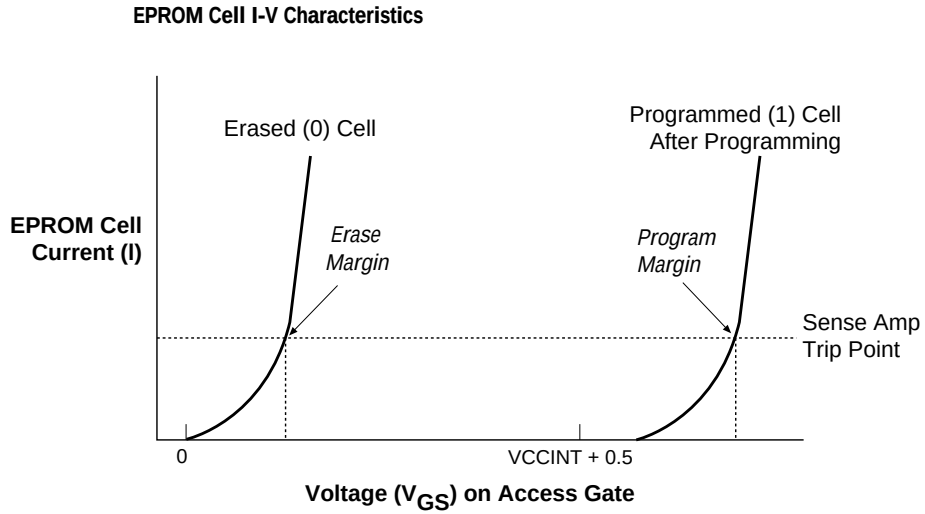


Figure 6 shows the current-voltage (I-V) relationships for programmed (high-threshold voltage) and erased (low-threshold voltage) EPROM cells. The programmed EPROM cell behaves as a transistor that is turned off, because source-drain current does not flow for access-gate voltages ranging from 0 to V_{CC}. In contrast, an erased cell produces source-drain current when its access gate is brought to approximately 1 V, like a transistor that is turned on.

Programmed EPROM cells in the off state are erased by exposing the device to ultraviolet (UV) radiation with wavelengths of 2,540 Å. The excess electrons on the floating gate absorb radiant UV energy, experience a rise in energy level above the 3.2-eV barrier, overcome the oxide-silicon potential barrier, and finally migrate into the substrate, where they are neutralized.

Figure 6. Current vs. Voltage Relationships of Erased & Programmed EPROM Cells



Reliability Information

Results from Altera's reliability monitoring program are published several times each year in the *Altera Reliability Report*. This report summarizes the test results for all Altera devices over a 15-month period. It includes detailed descriptions of the reliability tests, their implementation, and useful information about semiconductor reliability. For a copy of the latest reliability report, contact Altera Literature Services at (888) 3-ALTERA.